WBS 6.5 : Tile Calorimeter Management Overview

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Conceptual Design Review of the High luminosity LHC Detector Upgrades
National Science Foundation
Arlington, Virginia
March 8-10, 2016

USATLAS TileCal L2 Construction Mgr

- Mark Oreglia, Professor of Physics, The University of Chicago
- Has been a member of ATLAS and the Tile Calorimeter team from the beginning (1995)
- US ATLAS Level-2 Tile Calorimeter Upgrade Construction mgr
  - Was co-leader of the CERN Tile upgrade R&D effort 2012-15
  - Was USATLAS L2 manager for TileCal upgrade R&D 2012-15
  - Authored the TileCal section of the summer 2015 upgrade scoping doc
  - Currently assisting the TileCal Project Leader in orchestrating the upgrade
- Leads the R&D effort at UChicago to design and prototype front-end boards and main control boards for the upgraded electronics
- Previous Experiments: Crystal Ball (SLAC), CCFR (FNAL), OPAL (LEP/CERN)

Outline

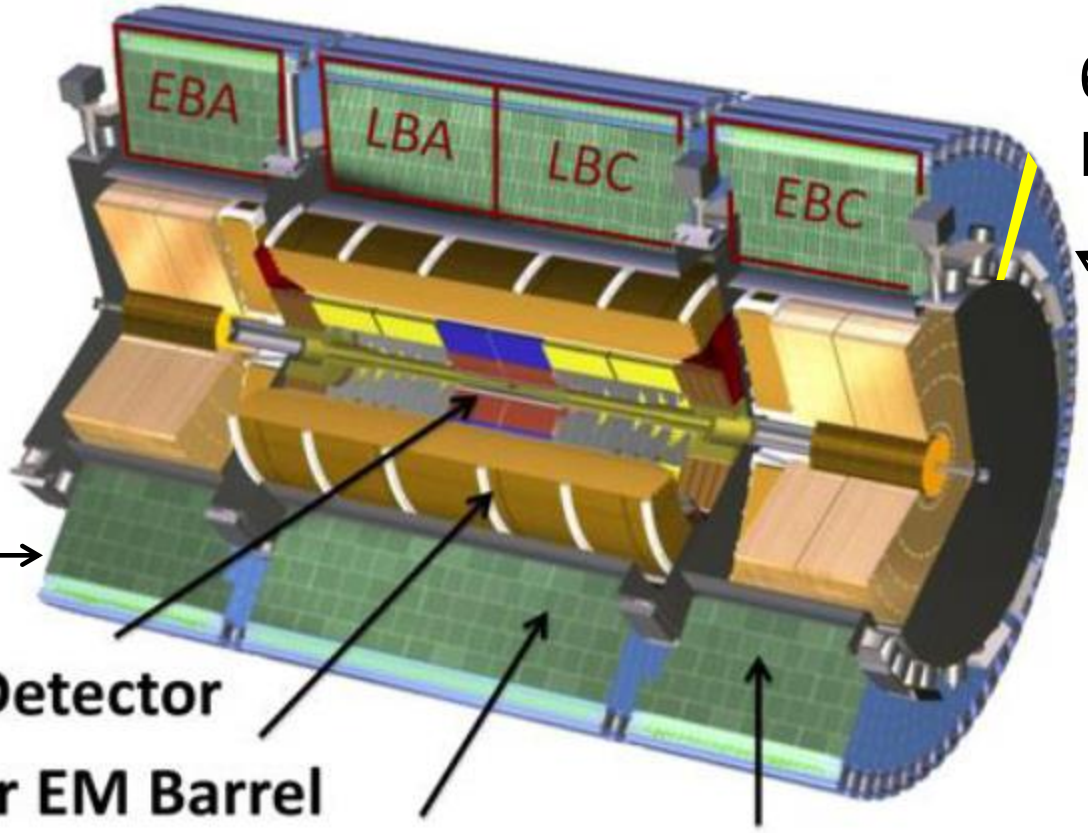
- Overview
  - Tile Calorimeter, Physics-driven upgrade, scope
- Organization
  - TileCal structure: International and US
- US Deliverables
  - Basis of estimation
- Costing
- Schedule
- Risk, Contingency
- List of BoEs

WBS 6.5: Tile Calorimeter

- This is the outer (hadronic) calorimeter
  - Preceded by LAr EM calorimeter
  - Steel/scintillator calorimeter measures ~35% of jet energy
- Upgrade institutions, WBS-L3, and subsystem managers:
  - University of Chicago, 6.5.1, (UC) Mark Oreglia
    - 6.5.1.1: Main Boards (MB of front-end electronics)
  - University of Texas/Arlington (UTA), 6.5.2, Kaushik De
    - 6.5.2.2: Preprocessor (PPR, back-end DAQ), Giulio Usai
    - 6.5.2.4: Low Voltage “bricks” (LVproduction), Haleh Hadavand
  - Michigan State university, 6.5.3, (MSU) Joey Huston
    - 6.5.3.3: ELMB++ Motherboards (ELMB-MB, LV system)
  - Northern Illinois University (NIU), 6.5.4, Dhiman Chakraborty
    - 6.5.4.2: Low Voltage “boxes” (LVassembly)

The Current Tile Calorimeter

4 “barrels”, 256 modules



64 ϕ Wedges
R: 2.28-3.87m

LV “finger” boxes

D Layer

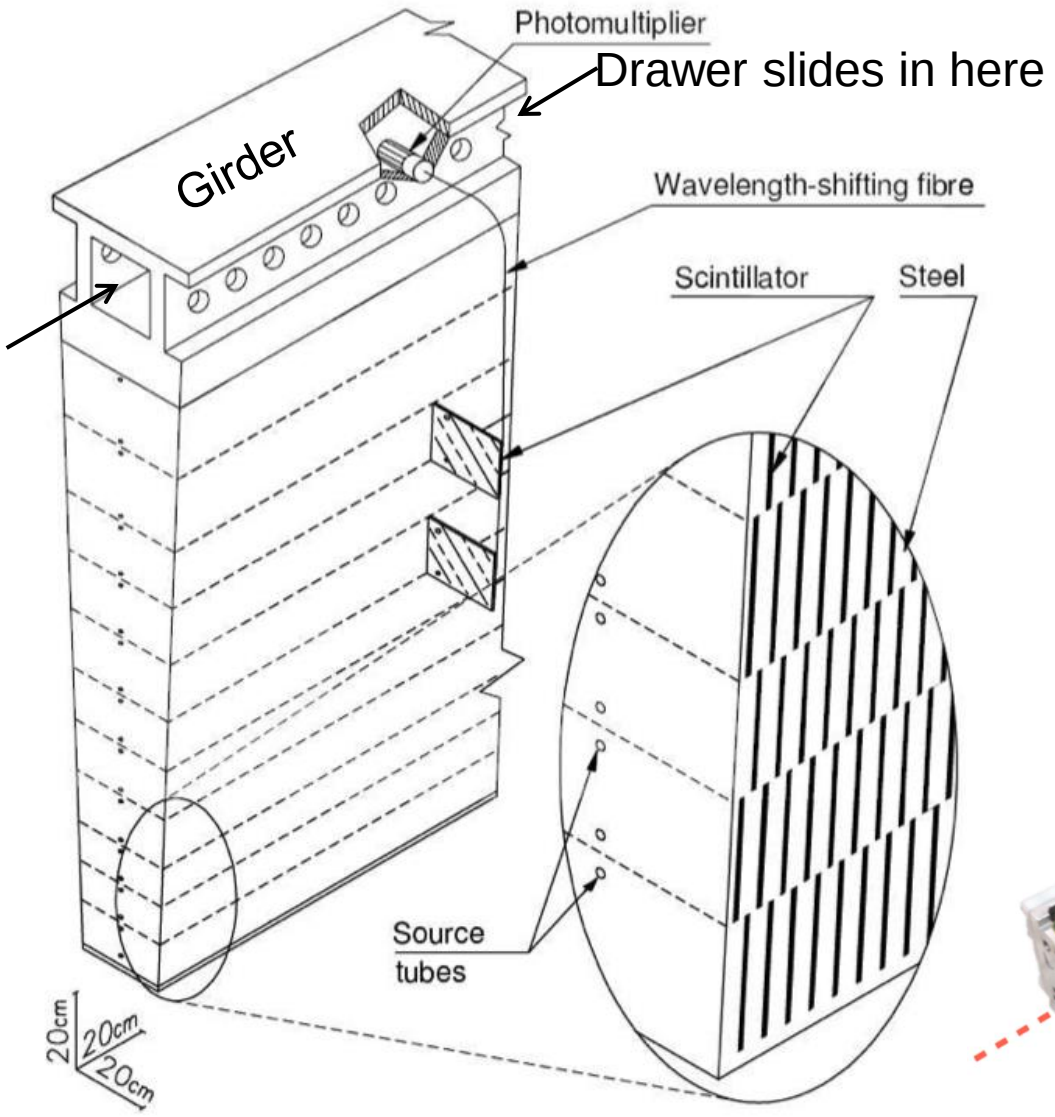
Inner Detector

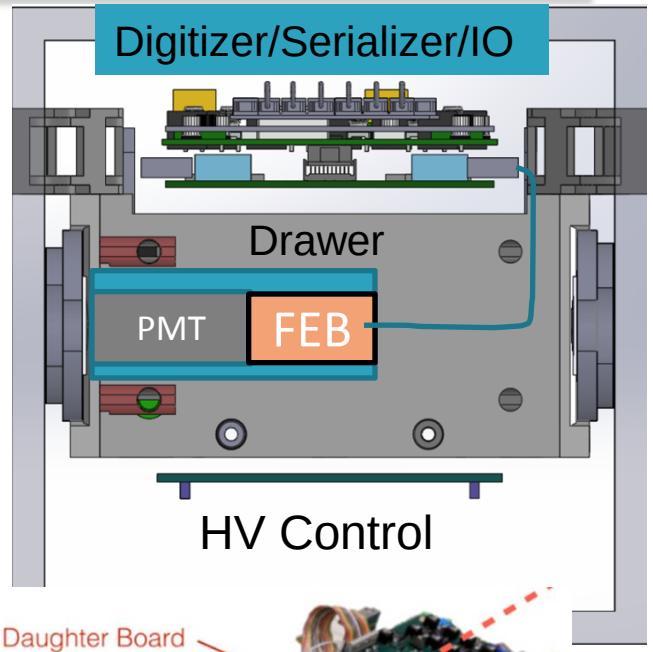
LAr EM Barrel

Tile Barrel

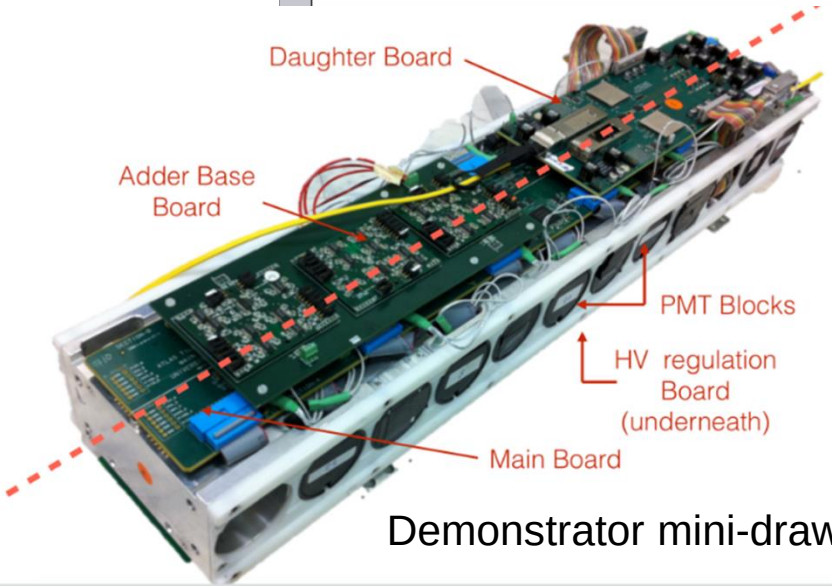
Tile Extended Barrel

Tile Wedge Structure





HV Control



Demonstrator mini-drawer

Physics ⇒ Technology

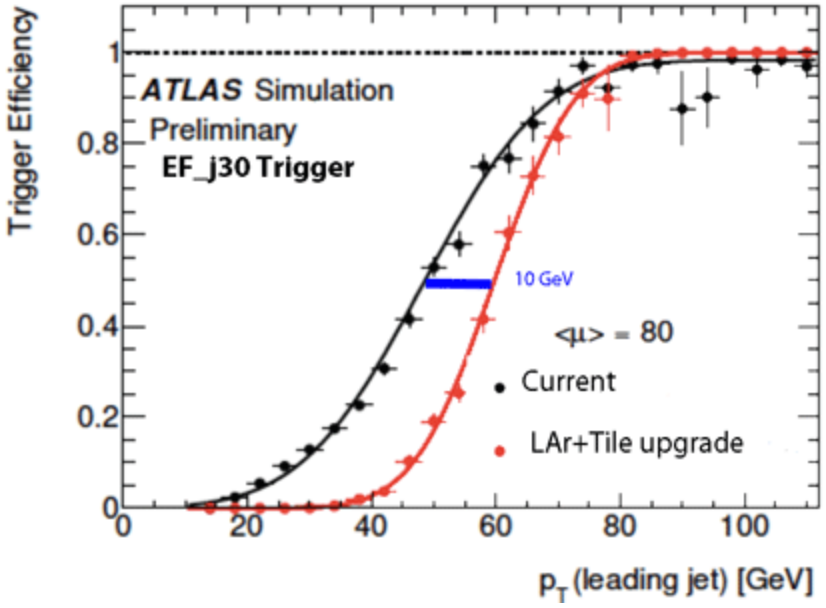
The Physics mission requires readout of the full granularity of Tile at the 1 MHz L0 trigger rate

SCIENCE GOALS	SCIENCE REQUIREMENTS	NSF SCOPE
$H \rightarrow 4\mu$ (2.2%) VBF $H \rightarrow ZZ^*, WW^*$ (17%,14%) VBS ssWW (5.9%) SUSY $\chi_1^{\pm} \chi_2^0 \rightarrow \ell bb+X$ (850 GeV)	Muon Trigger • single μ p_T threshold ~ 20 GeV • geometric accept: 95% (barrel)	• Muon Electronics • Tile Electronics • sMDT • L0Muon
VBF $H \rightarrow ZZ^*, WW^*$ (17%,14%) VBS ssWW (5.9%) SUSY $\chi_1^{\pm} \chi_2^0 \rightarrow \ell bb+X$ (850 GeV)	Electron Trigger • single e p_T threshold ~ 22 GeV	• LAr+Tile Electronics • L1Global • L1Track/FTK++
$HH \rightarrow 4b$ (4.4σ KK Graviton)	Jet Triggers • 4-jet E_T threshold ~ 75 GeV • "fat" jet threshold ~ 375 GeV • jet-vertex confirmation at L1	• Lar+Tile Electronics • L1Global • L1Track/FTK++
Compressed SUSY ($\chi_1^{\pm} \chi_2^0$)	Missing E_T Trigger • ME_T threshold ~ 200 GeV • track-based ME_T correction	• Lar+Tile Electronics • L1Global • L1Track/FTK++

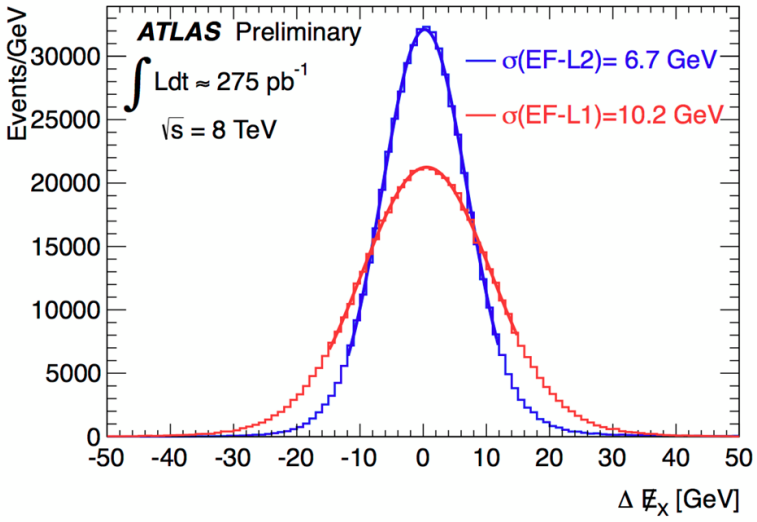
Cost-Effective Trigger System that meets Science Requirements:
- <L0 accept>=1 MHz (6/10μs); <L1 accept>=400 kHz (30/60μs); <to storage>=10 kHz

2 Examples: Physics Impact

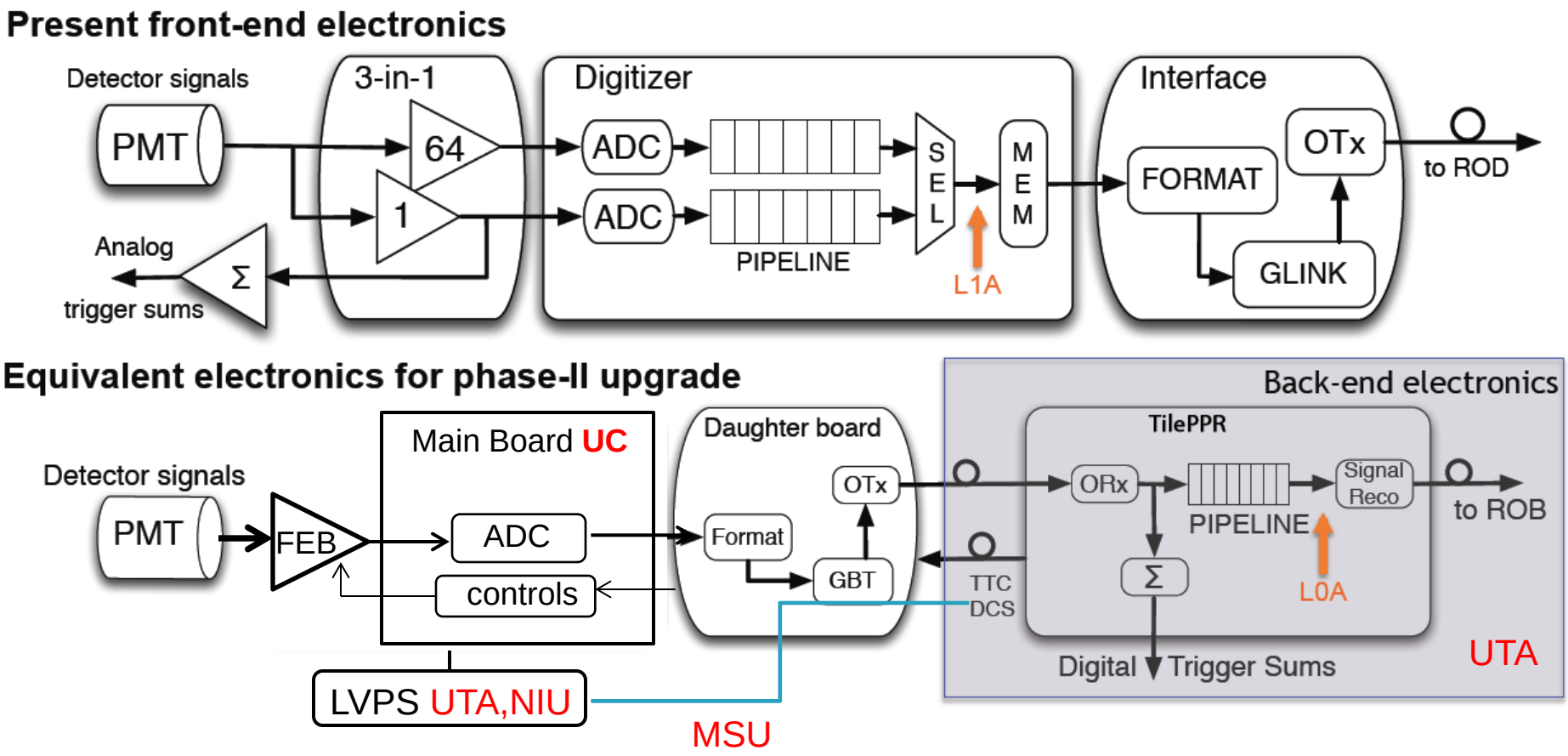
- Jet Trigger Rate
  - Energy resolution improved:
    - lower noise
    - better pileup handling
  - factor 10 improvement in trigger rate



- Missing Energy Resolution
  - Inability to read-out digital data at 40 MHz will hugely impact missing-Et and Ht triggers.
  - Here are distributions when missing-Et is calculated with the analog sums (L1) and digital data (L2):
  - You can see that the digital data gives much smaller noise to missing-Et.
  - The improvement is much higher at \mu=200.



New vs Old Electronics



NB: New electronics already prototyped (“Demonstrator”)

International ATLAS Tile Scoping, Identification of Expertise

- 2012 LOI and 2015 scoping established the full scope of needed Tile upgrade
- Tile Institute Board has agreed on undertaking of upgrade tasks by the traditional Tile institutions:

- good match between interest and expertise
- unofficial money-matrix covers the scope adequately
- Agreements on task sharing were made

Item	Intentions/Interests for production
Mini-drawers	Romanian cluster, IFAE, Clermont consulting
LVPS	UTA, Pisa, Prague AS and CU (ANL consulting), MSU (ELMB)
Active Dividers	To be found, Testbench to be handed by Clermont
FEB+MB	Chicago, Clermont shared In half in items (ANL consulting)
DaughterBoard	Stockholm
HV system	LIP, Prague AS and CU (to specify item) + Clermont help + ANL consulting(if HV opto)
TilePPr, i/f to TDAQ	Valencia, Wits, UTA
New DCS	LIP, MSU (also for ELMB developments)
PMT block	Dubna + to be found
PMTs robustness	Pisa, [Yerevan], UTA (have lifetime bench), Clermont
Optics	counters: Dubna, Wits, Protvino, CERN, MSU; fibers: LIP
MA-PMTs	Dubna, Minsk, CERN, Protvino, ANL(S.Ch), Pisa, MSU, UTA, synergies w/ ALFA
Laser system	Clermont (consulting), Pisa, LIP, CERN
Cs system	Protvino, CERN

US/NSF Deliverables

- 6.5.1.1 (UC): Main Boards of front-end system
  - designed old and new front-end systems (demonstrator)
- 6.5.2.2 (UTA-1): Pre-processor TDAQi (interface boards)
  - has expertise in original "ROD" preprocessor and development of demonstrator back-end electronics
- 6.5.3.3 (MSU): motherboards for LV control
  - experts on Detector Control Systems since the beginning
- 6.5.2.4 (UTA-2): LV Power System (50% of LV "bricks")
- 6.5.4.4 (NIU): LV Assembly (50% of LV "boxes")
  - US redesigned LV system after original system started failing; vast improvement

ATLAS WBS	ATLAS Item (Scoping Doc)	US WBS	Deliverable	NSF Fraction Design	NSF Fraction Production
4	**Tile Calorimeter**	**6.5**	**Tile Calorimeter**		**21%**
4.1	**Drawer Mechanics**				**-**
4.1.1	Mini-drawers				-
4.1.2	Tools/Mechanics				-
4.2	**On-detector Electronics**				**32%**
4.2.1	PMT Dividers				-
4.2.2	FE Boards				-
4.2.3	Main Boards	6.5.1.1	Main Boards	100%	100%
4.2.4	Daughter Boards				-
4.2.5	LVPS System				53%
	ELMB++				-
	ELMB++ Motherboards	6.5.3.3	ELMB++ Motherboards	100%	100%
	LVPS	6.5.x.4	LVPS	100%	50%
4.2.6	HV System				-
4.3	**Off-detector Electronics**				**18%**
4.3.1	TilePPR				-
	TilePPr				-
	Tile TDAQi	6.5.2.2	TDAQi	100%	100%
4.4	**Infrastructure**				**-**
4.4.1	Services				-

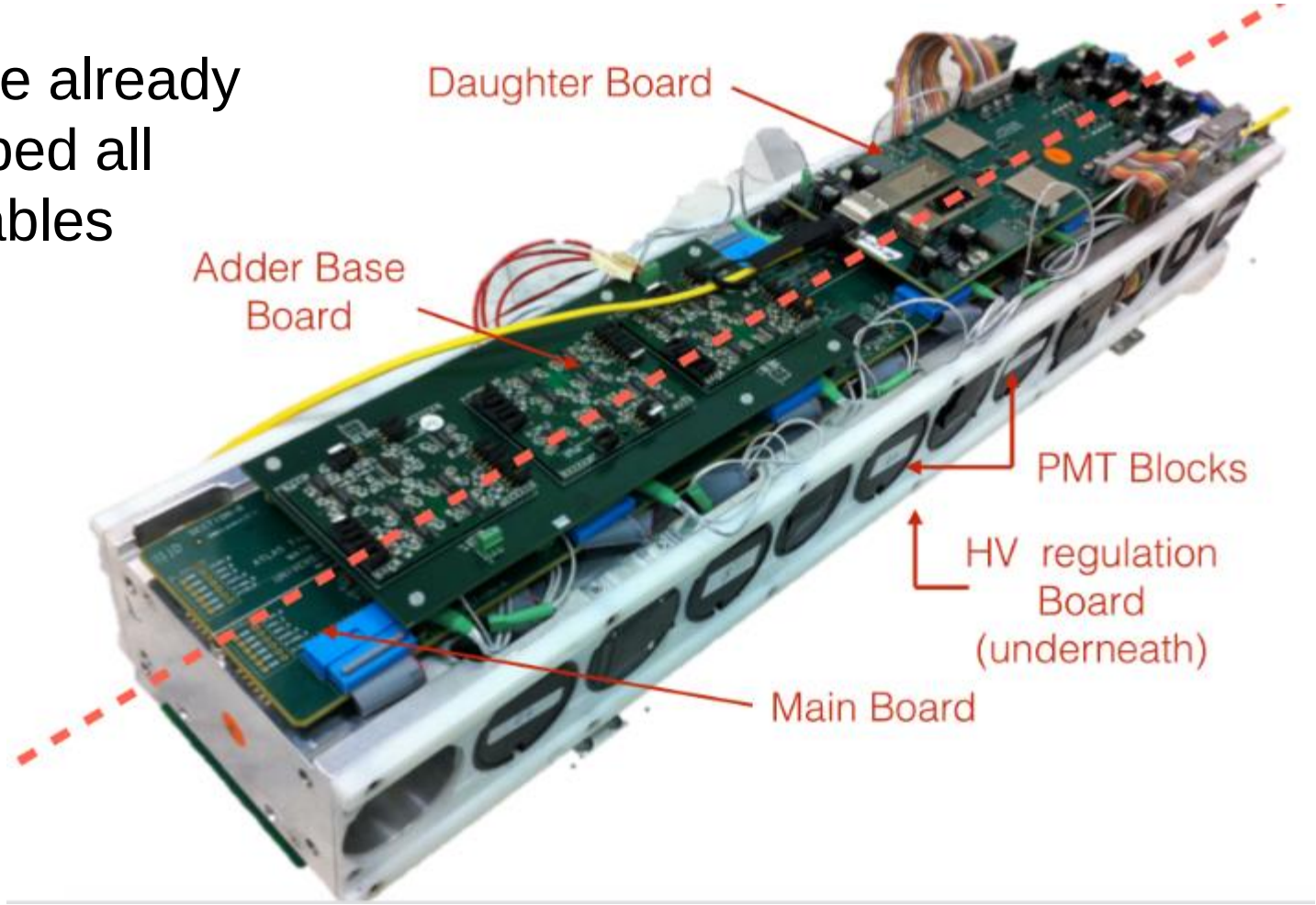
Organizational Structure

- International TileCal:
  - Institute Board: lead representatives from each contributing institution; meets 3 times per year and for ad hoc issues
  - Upgrade R&D group: co-leaders coordinate the R&D for construction and testing of a demonstrator; meet approx. 4 times per year for "Expert Weeks"
- USATLAS:
  - Level-2 Tile R&D Manager (A. Paramonov) coordinates R&D on US deliverables; scrubbing meetings with USATLAS management anually. Progress reports quarterly to USATLAS.
  - Level-2 Tile Production Manager (M. Oreglia) liases with Tile Project Leader, CERN R&D managers, ATLAS Upgrade Steering group, USATLAS R&D manager. Coordinates construction of US deliverables and reports to USATLAS.

Before I describe costing:
A Demonstrator Mini-drawer

2 versions, 10 units fabricated to date

We have already prototyped all deliverables



Cost and Effort Estimates

(more details in the BOEs)

- For MB, ELMB-MB, and LV: upgrade is essentially the old system with new components, thus very good check on cost estimate
- The cost estimates are rather detailed and based on production of several demonstrator prototypes
  - actual or similar Bill of Materials with quotes from vendors for FY18
  - effort estimates based on the original construction, refined by the recent experience building and testing boards for the demonstrator
    - The FEB, Main Boards, LVPS bricks and boxes are very similar in production scope to the current versions … which we built!
    - The PreProcessor cards are new, ATCA technology, but we have the experience of constructing the demonstrator prototypes
- The method of estimation is therefore a combination of
  - Engineering Build-Up: PPR, ELMB-MB
  - Extraplolate from Actuals: MB, LV

Cost Profile by Task

6.5 Tile Calorimeter NSF Total Cost by Phase (AYk$)						
Deliverable/Item/Phase	FY20	FY21	FY22	FY23	FY24	Grand Total
6.5.1 Tile_Chicago	**592**	**856**	**277**	**32**	**33**	**1,790**
6.5.1.1 Main Board	**592**	**856**	**277**	**32**	**33**	**1,790**
Production Procurement	456	456	0	0	0	912
Production PCB Assembly	136	137	0	0	0	274
Production Burn-in	0	175	180	0	0	355
Production Diagnose & Repair	0	37	38	0	0	75
Ship to CERN	0	20	27	0	0	47
Accceptance Test	0	31	31	8	8	77
Management	0	0	0	24	25	49
6.5.2 Tile_UTA	**461**	**581**	**313**	**65**	**0**	**1,421**
6.5.2.2 Preprocessor	**65**	**262**	**232**	**65**	**0**	**623**
Pre-Prod Parts Procurement/QA	31	0	0	0	0	31
Pre-Prod PCB Assembly, QA	19	0	0	0	0	19
Pre-Prod Board Testing	15	0	0	0	0	15
Parts Procurement/Q&A	0	113	110	0	0	223
PCB Assembly, QA	0	20	8	0	0	28
Burn-in	0	63	52	31	0	147
Repairs	0	65	62	22	0	148
Shipping	0	0	0	12	0	12
6.5.2.4 Low Voltage Power Supply	**397**	**320**	**82**	**0**	**0**	**798**
Pre-prod Parts Procurement	39	0	0	0	0	39
Pre-prod PCB Fab and Assy	19	0	0	0	0	19
Pre-prod Basic Checkout and Burn-in	34	0	0	0	0	34
Pre-prod Repairs	21	0	0	0	0	21
Pre-prod Test Equipment	19	0	0	0	0	19
Parts Procurement	119	122	0	0	0	240
PCB Fabr & Assy	67	61	0	0	0	128
Basic Checkout & Burn-in	54	92	50	0	0	196
Repairs	11	20	19	0	0	50
Management	11	22	11	0	0	44
Shipping	2	3	2	0	0	7
6.5.3 Tile_MSU	**84**	**80**	**90**	**78**	**0**	**332**
6.5.3.3 ELMB++ Motherboards	**84**	**80**	**90**	**78**	**0**	**332**
Pre-Prod Burn-in, Test & Repair	84	0	0	0	0	84
Parts Procurement/Q&A	0	44	44	0	0	88
Burn-in/Test/Repair	0	33	41	73	0	147
Shipping	0	3	4	5	0	12
6.5.4 Tile_NIU	**144**	**203**	**42**	**56**	**0**	**446**
6.5.4.4 LVPS Assembly	**144**	**203**	**42**	**56**	**0**	**446**
Final Design	48	0	0	0	0	48
Pre-Prod Procurement	63	0	0	0	0	63
Pre-Prod Assembly	11	0	0	0	0	11
Pre-Prod Burn-in, Test & Repair	15	0	0	0	0	15
Pre-Prod Diagnostics & Repair	7	0	0	0	0	7
Test Equipment	0	64	0	0	0	64
Production Procurement	0	139	0	0	0	139
Production Assembly	0	0	11	2	0	14
Production Burn-in/Checkout	0	0	14	14	0	28
Production Diagnose & Repair	0	0	17	18	0	35
Shipping	0	0	0	22	0	22
NSF Grand Total	**1,282**	**1,720**	**723**	**231**	**33**	**3,988**

6.5.1.1 Main Board

- Production Procurement
- Production PCB Assembly
- Production Burn-in
- Production Diagnose & Repair
- Ship to CERN
- Accceptance Test
- Management

Main Board Costing

- Commercial components; have BOM and quotes
  - Assume 20% discount from retail based on much experience
- Complex PCB assembly; have experience with assembly firm, and production quote
  - Yield assumed at >90% based on demonstrator
- Labor and schedule estimated from both recent demonstrator experience and original cost book from production of current motherboards
  - Very similar burn-in procedure and same number of boards

WBS	Deliverable	FTE	Labor	M&S	Travel	Total
6.5.1.1	Main Boards	5.2	$648,939	$1,109,614	$31,340	$1,789,893

TDAQi Costing

- This component not precisely prototyped for demonstrator
  - But architecture has been established (based on flexibility achievable using an advanced FPGA)
  - Have BOM and experience assembling similarly complex PCB for demonstrator
- Labor estimated from extrapolation from original “sROD” production

WBS	Deliverable	FTE	Labor	M&S	Travel	Total
6.5.2.2	Preprocessor	3.5	$358,306	$241,600	$23,130	$623,036

ELMB Motherboard Costing

- Extremely similar to current system
- Component and board costs based on cost of old system
- Labor estimate taken from actual effort in producing old system

WBS	Deliverable	FTE	Labor	M&S	Travel	Total
6.5.3.3	ELMB++ Motherboards	1.6	$211,185	$66,360	$54,120	$331,665

LV System Costing

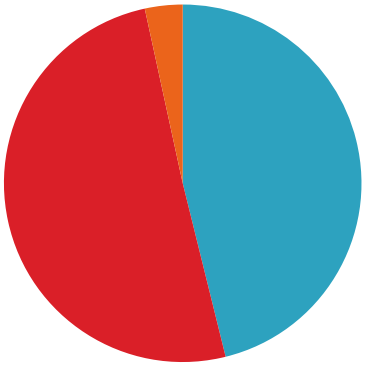
- Based on production of 48 units for demonstrator
  - and production of 2100 similar units in current system
- New design is minor modification of existing system
  - Completely replaced on current ATLAS detector in 2014, so have recent experience in cost and effort
  - Well documented (see BoE)

WBS	Deliverable	FTE	Labor	M&S	Travel	Total
6.5.2.4	LVPS Production	6.0	$389,342	$400,767	$8,000	$798,109
6.5.4.4	LVPS Assembly	1.4	$232,419	$193,950	$19,275	$445,644

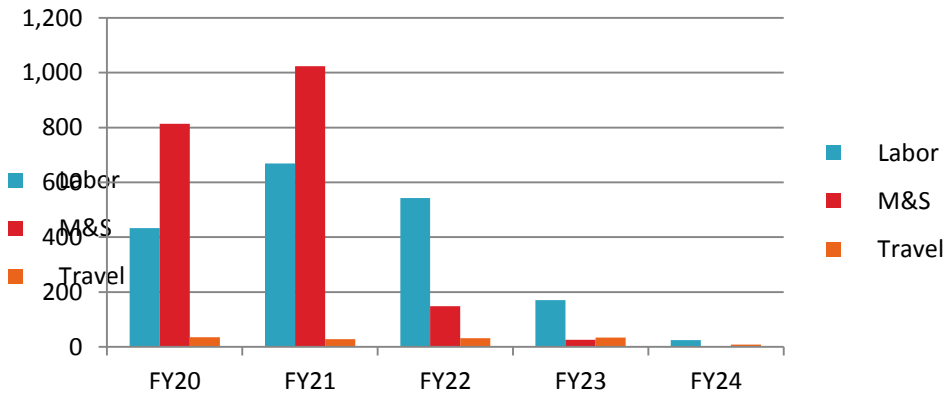
L2 Total Cost

6.5 Tile Calorimeter NSF Total Level 2 Cost (AYk$)						
	FY20	FY21	FY22	FY23	FY24	Grand Total
NSF						
Labor	433	669	542	171	25	1,840
M&S	814	1,023	149	26	0	2,012
Travel	35	28	32	34	8	136
NSF Total	**1,282**	**1,720**	**723**	**231**	**33**	**3,988**

WBS 6.5 Tile Calorimeter L2 NSF Resource Breakdown



WBS 6.5 Tile Calorimeter L2 NSF Fiscal Year Costs AYk$



Effort

No new effort!

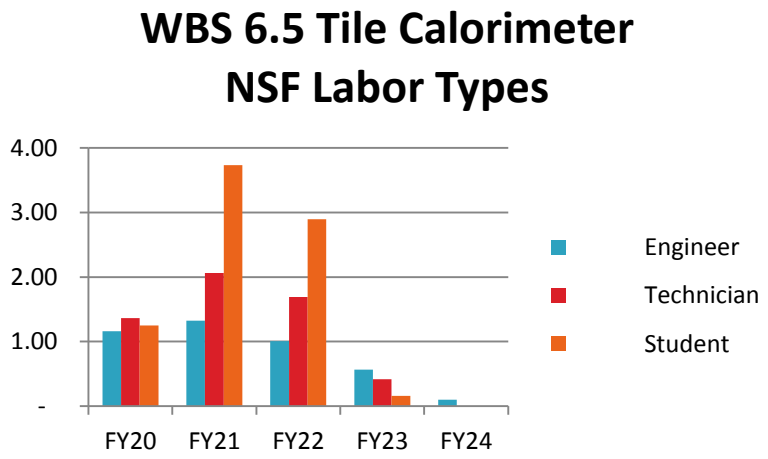
Accurate estimate from similar task constructing original detector

6.5 Tile Calorimeter NSF Total FTEs by Deliverable						
Deliverable/Item	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Grand Total**
Main Board	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
6.5.1.1 Main Board	0.30	2.45	2.20	0.10	0.10	5.15
Preprocessor	**0.26**	**1.44**	**1.36**	**0.42**	-	**3.48**
6.5.2.2 Preprocessor	0.26	1.44	1.36	0.42	-	3.48
ELMB++MB	**0.45**	**0.37**	**0.47**	**0.35**	-	**1.64**
6.5.3.3 ELMB++MB	0.45	0.37	0.47	0.35	-	1.64
LVPS	**2.77**	**2.86**	**1.55**	**0.27**	-	**7.45**
6.5.2.4 LVPS	2.23	2.51	1.28	-	-	6.02
6.5.4.4 LVPS Assembly	0.54	0.35	0.27	0.27	-	1.42
NSF Grand Total	**3.78**	**7.12**	**5.59**	**1.14**	**0.10**	**17.72**

Labor by Type

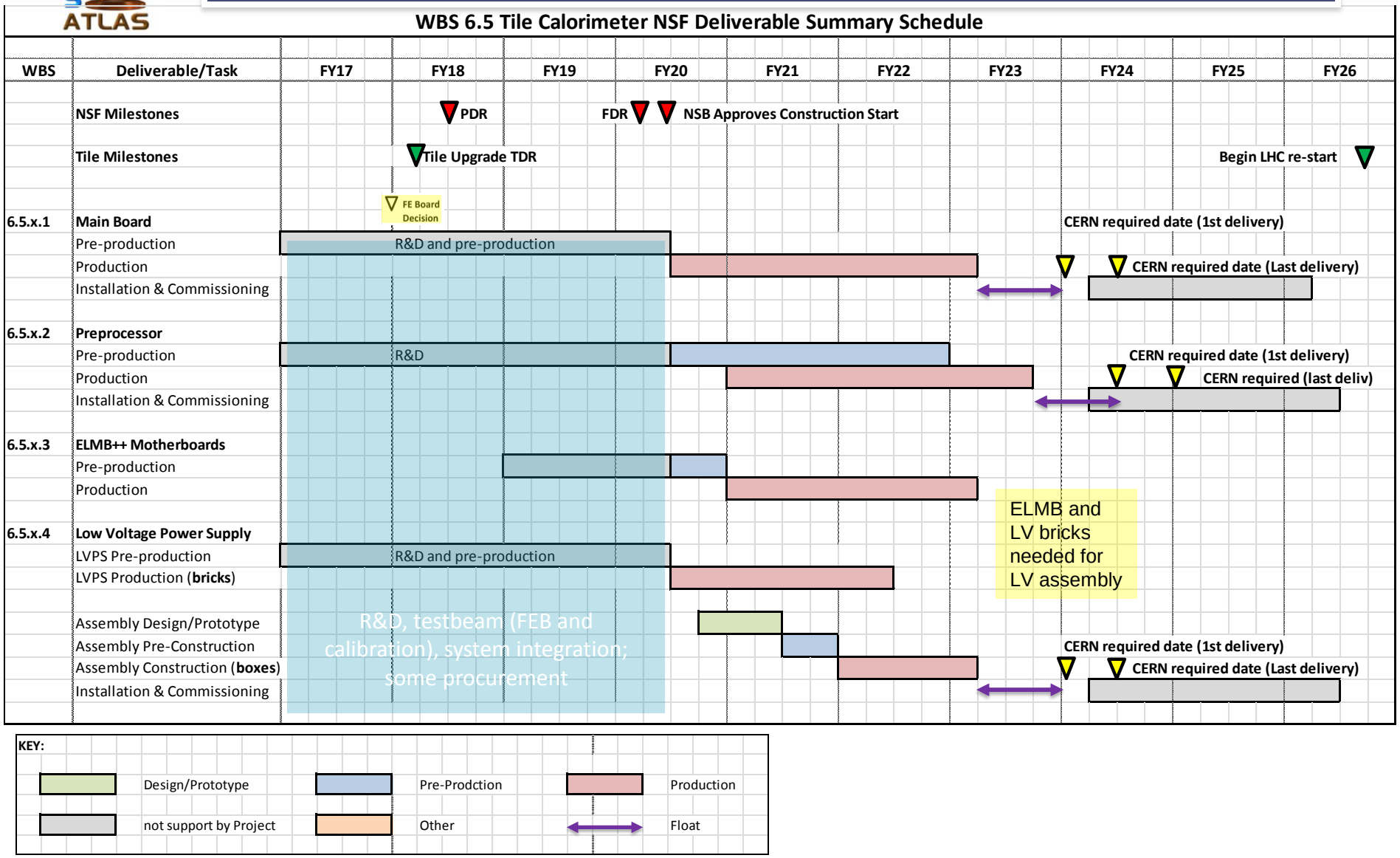
6.5 Tile Calorimeter NSF Total FTEs by labor type						
Deliverable/Item/Labor Type	FY20	FY21	FY22	FY23	FY24	Grand Total
6.5.1 Tile_Chicago	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
6.5.1.1 Main Board	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
Engineer	0.10	0.50	0.40	0.10	0.10	1.20
Technician	0.20	0.95	0.80	-	-	1.95
Student	-	1.00	1.00	-	-	2.00
6.5.2 Tile_UTA	**2.49**	**3.95**	**2.64**	**0.42**	**-**	**9.50**
6.5.2.2 Preprocessor	**0.26**	**1.44**	**1.36**	**0.42**	**-**	**3.48**
Engineer	0.26	0.40	0.32	0.16	-	1.14
Technician	-	0.52	0.52	0.26	-	1.30
Student	-	0.52	0.52	-	-	1.04
6.5.2.4 Low Voltage Power Supply	**2.23**	**2.51**	**1.28**	**-**	**-**	**6.02**
Engineer	0.11	0.17	0.08	-	-	0.36
Technician	0.87	0.35	0.20	-	-	1.42
Student	1.25	2.00	1.00	-	-	4.25
6.5.3 Tile_MSU	**0.45**	**0.37**	**0.47**	**0.35**	**-**	**1.64**
6.5.3.3 ELMB++ Motherboards	**0.45**	**0.37**	**0.47**	**0.35**	**-**	**1.64**
Engineer	0.23	0.10	0.11	0.24	-	0.68
Technician	0.23	0.06	0.08	0.04	-	0.41
Student	-	0.21	0.28	0.07	-	0.56
6.5.4 Tile_NIU	**0.54**	**0.35**	**0.27**	**0.27**	**-**	**1.42**
6.5.4.4 LVPS Assembly	**0.54**	**0.35**	**0.27**	**0.27**	**-**	**1.42**
Engineer	0.47	0.16	0.09	0.07	-	0.78
Technician	0.07	0.19	0.09	0.11	-	0.46
Student	-	-	0.09	0.09	-	0.18
NSF Grand Total	**3.78**	**7.12**	**5.59**	**1.14**	**0.10**	**17.72**
Engineer	1.16	1.32	1.01	0.57	0.10	4.16
Technician	1.37	2.06	1.69	0.42	-	5.53
Student	1.25	3.73	2.89	0.16	-	8.03

As these Tile projects are at universities, we benefit from low-cost labor by **undergrads**: it's good experience for them! They are qualified to monitor the burn-in and testing.



Level 4 Timeline

Driven by CERN Scoping Document and installation schedule



External Dependencies

no showstoppers

- MB: burn-in to be done with front-end cards supplied by Clermont
  - Could use cards from demonstrator for MB production
- PPR: - no external dependency –
- ELMB Motherboard: needs ELMB++ chip supplied by ATLAS
  - Could run motherboard testing using ELMB++ surrogate
- LV system: LV box chassis and cold plate supplied by Prague
  - can restructure procurement to make those parts in US for 50% of boxes

System Integration

- Gary Drake, EE at UC and ANL, has been asked to act as Integration Engineer for Tile
  - He has long-time knowledge of Tile electronics
  - He designed and produced the new LV system in current detector
  - Since 2012 he has been the Project Manager for the CERN Tile Upgrade R&D (Demonstrator Project)
- Gary's contributions were am important reason for the progress and success we have had in the demonstrator project
- Main Responsibilities:
  - Organize "Expert Weeks" during R&D and pre-production era
  - Organize reviews of final design and check that CERN requirements have been satisfied
    - TDAQ specs; radiation certification
  - Monitor schedule, identify problems and ensure they are addressed
  - Interact with international ATLAS/Tile
  - Oversee delivery to CERN and acceptance testing

Risks

- Risks all low because of working demonstrator prototype
- Cost risk: very low
  - have BOMs from demonstrator; cost goes down for CERN bulk purchases
  - only assuming 20% bulk discount from retail (it's usually higher)
  - FPGAs likely to go down in cost; we are using quotes for FY18
- Schedule risk: low
  - not negligible, because Tile installation is early in the schedule
  - but significant float in proposed schedule (12-19 months)
- Technical risk: very low
  - Tile is in lower radiation area
  - electronics design not too sophisticated; often similar to current design
  - main risk: replacement component does not meet radiation standard

Budget Contingency (1)

- 35% for low-risk system, rather conservatively applied:
  - Material Contingency Rule 4 :
    - "25-40% contingency on: items that can be readily estimated from a reasonably detailed but not completed design; items adapted from existing designs but with minor modifications, produced within the previous two years, with documented costs. A recent vendor survey based on a preliminary design belongs here."
    - In fact, parts quotes exist, but purchases to be made in FY20,21.
  - Labor Contingency Rule 3:
    - "25-40% contingency for a task that is conventional, well defined and tends to be repeatable with good confidence but can expect small fluctuations; .for example, testing of production electronics components (most boards take the same unit time, a few take longer); for example, fabrication of multiple similar components but which are not an assembly-line process; for example, design labor for conventional items which offer little to no technical risk."
    - Effort estimate is solid, but assume 2.5% inflation in rates

Budget Contingency (2)

- MB: have BOM's and good estimate of effort from demonstrator (production of 10 Main Boards); supported by actual labor for original motherboard production at UC
- PPR/TDAQi: have good estimate of BOM from PPR+TDAQ demonstrator prototype. Effort well estimated from original ROD production.
- ELMB-MB/DCS: very similar to existing motherboard, and have detailed production estimate from lead engineer.
- LV System: production effort and material virtually identical to 2014 replacement of current LV system. Well documented production plan.

Scope Contingency

- Decision to be made by management, consultation with Int'l ATLAS
- For all subsystems, by late FY21 we will know:
  - actual parts cost
  - failure rate ⇒ repair effort
- If infusion of funds not possible from contingency or Int'l ATLAS:
  - LV box/assembly production 6.5.4.4 would be the easiest deliverable to hand over:
    - comes as last electronics effort; last step in LV system chain
    - most likely US task to find someone else to cover – expertise at Prague
    - recovers $397k (11%)
    - would need to make that decision in CY 2021

Scope Opportunity

- Scope Opportunity … decided by US management
  - LVPS: there are arguments for building 100% in US
    - US undertakes 50% production in current proposal
    - US has proven track record for this
    - Achieve better product consistency
    - Would cost additional $1063K
    - BUT … decision would have to be made by FY21
  - Main Board, if 3in1 front-end board is not chosen:
    - for ASIC FEB the MBs are simpler, cheaper
    - could use the cost recovered to contribute FEB test stands, etc
      - decision by FY21
    - again, a decision to be made by management
    - approximate cost recovery: ~ $400k

“What if?” Scenarios

- Not issues:
  - Tile Calorimeter upgrade is in all CERN scoping scenarios
  - Currency (€,CHF/$): all purchases from US suppliers
- MB: FEB downselect: decide whether to engage in FEB testing
  - becomes a scope opportunity issue
- Certain parts become unavailable
  - all subsystems use very common components; alternatives will exist
- Critical parts are no longer pass radiation certification
  - not too big an issue, but modest additional cost for re-certification
  - main players: DC-DC converters, FPGAs/microcontrollers, ADCs
    - CERN working on common radiation tolerant DC-DC converters
    - rad-tolerant ADCs being designed by other groups
    - can use fusable microcontrollers
- LHC schedule delay
  - minor impact on parts costs (~inflation)
  - possibility of losing some expert personnel, but they can be replaced
    - only conventional EE skillset needed; project is well documented

BoE List

- 6.5.1.1 MB: UC
- 6.5.2.2 PPR/ TDAQi: UTA
- 6.5.3.3 ELMB motherboard/DCS: MSU
- 6.5.2,4.4 LV System
  - 6.5.2.4 LV “bricks”: UTA
  - 6.5.4.4 LV “boxes” and assembly: NIU

Closing Remarks

- US Deliverables: Main Boards, PPR TDAQi, ELMB-MB/DCS, LVPS
  - developed by US groups with long-time involvement in Tile
  - already proven by Tile demonstrator project
    - costs and effort well understood ⇒ low risk and well within contingency
- Total construction cost of $3988K (w/o contingency)
  - 2.8% of total US projects
- Low risks; here are the main ones, all mitigable:
  - MB: new component not radiation tolerant
  - PPR: FPGA cost
  - ELMB motherboard: new component not radiation tolerant
  - LVPS: new component not radiation tolerant

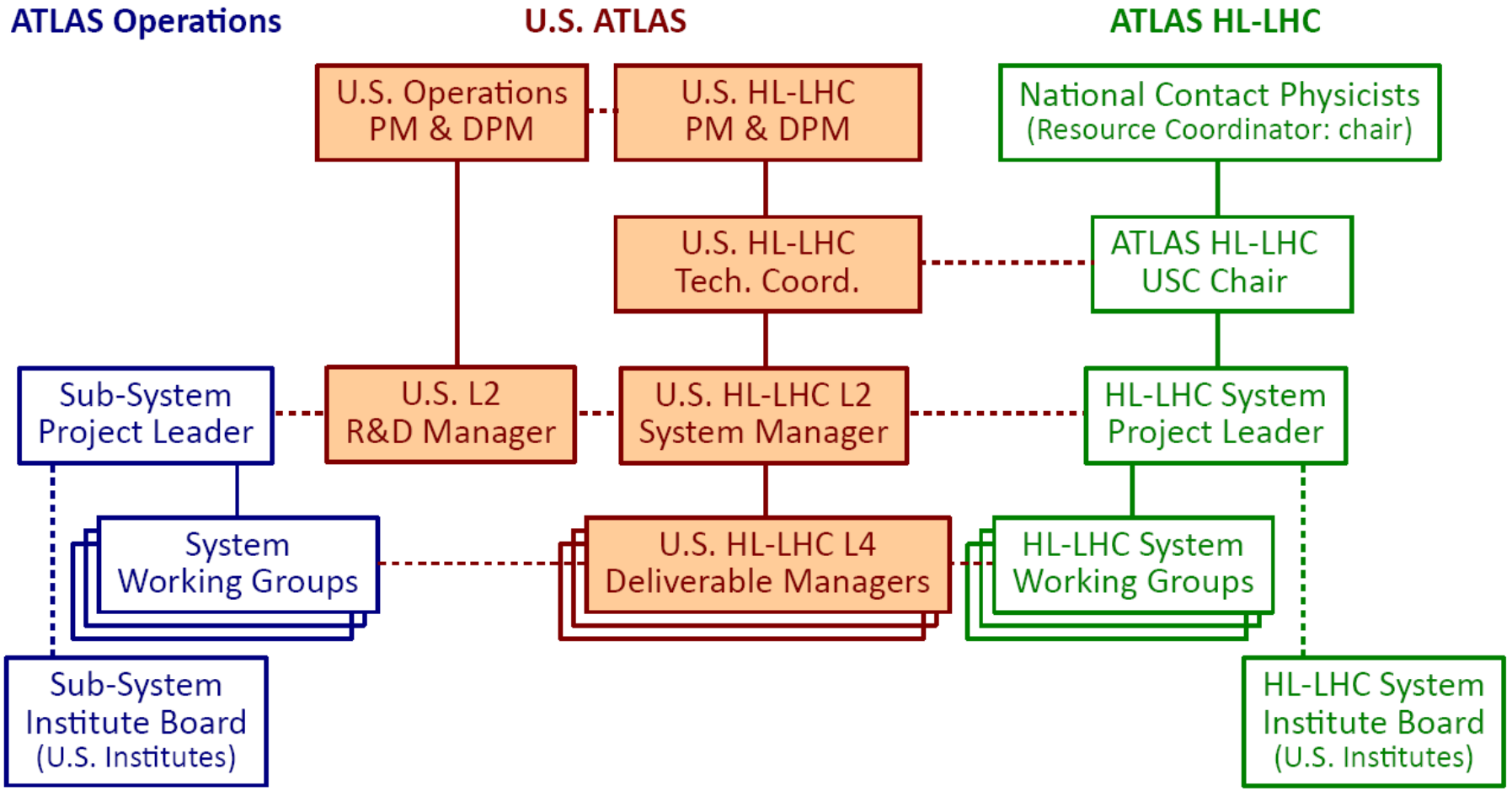
Backup Slides

- More Physics and Technical Motivation
- Organizational Interactions
- WBS Definitions 6.5.x.1,2
- WBS Definitions 6.5.x.3,4
- Cost Profile by Deliverable
- 6.5.1.1: Main Board (UC)
- 6.5.2.2: Pre-Processor TDAQi (UTA-1)
- 6.5.3.3: ELMB++ Motherboard (MSU)
- 6.5.x.4: LVPS (UTA,NIU)
- Front-end Alternatives: Pending Downselect
- Schedule from Scoping Document
- 6.5 Risk Registry
- L3 Total Cost by Institution
- Effort: FTEs by Task

More Physics and Technical Motivation

- Physics Motivation:
  - Energy resolution impacts jet rates and physics analysis:
    - ~400MeV noise on current copper trigger lines $\Rightarrow$ optical Tx
    - pileup: get better resolution by storing energies from all cells
      - get longitudinal profile too
  - Missing Energy: dead cells bad for searches
    - increase redundancy and reliability
    - reduce Single Event Upsets
  - Trigger: use information from all cells and configure smart fast triggers in back-end
  - Therefore, send all cell data off-detector: requires new front- and back-end electronics
- Technical Motivation:
  - Radiation: harden electronics, increase redundancy
    - Each drawer ϕ-half completely independent, has separate:
      - 10 volt feed, FPGA and uplink; one half can take over from the other
    - ALARA-driven safer drawer mechanics: 69cm units instead of 140cm
  - Configurable Trigger
    - Send all cell energies to pre-processor
  - NB: the scintillator tiles and PMTs do not require upgrade

Organizational Interactions



WBS Definitions 6.5.x.1,2

WBS #	WBS Title	WBS Dictionary	Level 2 Manager	Collaborating Institution	Funding Source
6.5	Tile Calorimeter	Replacement of readout and associated electronics for the Tile Calorimeter. US deliverables include: develoment of the Main Board, which houses front-end readout electronics; design and construction of data I/O transition modules for use with the Tile Pre-Processor boards; ELMB++ motherboards used in the collection of monitoring data from the detector and electronics; and production and assembly of the TileCal Low Voltage Power Supply system.	M. Oreglia (Chicago)	-	-
WBS #	WBS Title	WBS Dictionary	Deliverable PI	Collaborating Institution	Funding Source
6.5.1.1	Main Boards	This WBS covers the fabrication of main boards (MB) which manage the data flow, power distribution, monitoring, and calibrations of the Tile Calorimeter front-end electronics. This MB is more radiation tolerant than the current ones, which is a requirement for HL-LHC running. The deliverable for WBS 6.5.1.1 is production of 1,100 boards. Additional tasks are parts procurement and monitoring of outsourced assembly, elevated temperature burn-in of cards with testing and repair, and assembly on the "drawer" mechanical structure for acceptance testing at CERN.	M. Oreglia (Chicago)	Chicago	NSF
6.5.2.2	Preprocessor Interface Boards	This WBS covers the design and fabrication of the Trigger DAQ interface (TDAQi) blades which are the rear transition modules of the Tile calorimeter back-end preprocessor (PPR). These boards configure the processed data from the front-end electronics and route data to the DAQ system via the FELIX module and to the L0/L1 Calo and Muon trigger system through dedicated links. The deliverable for WBS 6.5.2.2 is production of 32 boards. Additional tasks are parts procurement and monitoring of outsourced assembly, burn-in of cards in a dedicated setup with validation testing and repairs when needed.	K. De (UTA)	UTA	NSF

WBS Definitions 6.5.x.3,4

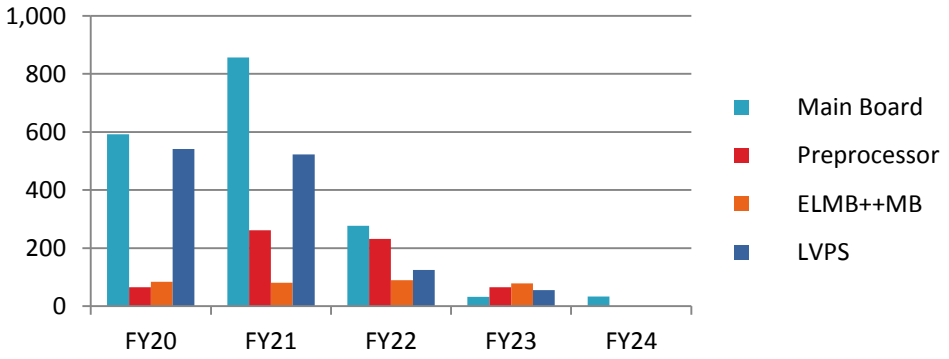
WBS #	WBS Title	WBS Dictionary	Deliverable PI	Collaborating Institution	Funding Source
6.5.3.3	ELMB++Motherboard	This WBS covers the design and fabrication of the motherboard for the new ELMB++ board to be designed for the Tilecal HL-LHC running. The ELMB++ (and its motherboard) is an integral part of DCS control for the Tilecal. The plan is for the new ELMB++ board to allow for greater diagnostic capability for Low Voltage Power Supply failures. The new motherboard, which is mounted in the LV finger box, has to be capable of supporting those new features. The deliverables for WBS 6.5.3.3 are: (1) design of a new motherboard, (2) prototyping of that board, (3) design and production of test equipment for the motherboard, (4) production of 256 ELMB++ motherboards boards over a two-year period, and (5) follow-up of the integration of the ELMB++ motherboards in the Tilecal LVPS system. Items 1 and 2 are not part of project costs, but will be covered by prototyping/R&D funding. Additional tasks are parts procurement and monitoring of outsourced assembly, elevated temperature burn-in of cards with testing and repair.	J. Huston (MSU)	MSU	NSF
6.5.2.4, 6.5.4.4	Low Voltage Power Supply	This WBS covers the production of the Low Voltage Power Supply for the ATLAS Tile Calorimeter HLLHC upgrade. This version of the LVPS consists of +10 volt modules (bricks); 8 of these bricks are mounted in LVBOXes which are mounted at the end of each Tile Calorimeter drawer. 256 of these boxes are needed for the full calorimeter. The primary deliverable for WBS 6.5.2.4 is production of half (1040) of the total number of bricks and half (130) of the LVBOXes ; about 1,140 bricks are produced to account for anticipated yield of 90% over a two-year period. Additional tasks include parts procurement, PCB assembly (outsourced), testing of the bricks at standard and elevated temperature (Burn-in), and repair of faulty bricks. The bricks will be shipped to NIU for inclusion in boxes of eight, tested and shipped to CERN. A transition period from ANL to UTA including	A. Brandt (UTA) H. Hadavand (UTA) D. Charaborty (NIU)	UTA UTA NIU	NSF NSF NSF

Cost Profile by Deliverable

- front-loaded by procurement bulk purchases and test fixture construction
  - permits construction with ample float and maximal discount

6.5 Tile Calorimeter NSF Total Cost by Deliverable (AYk$)						
Deliverable/Item	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Total**
Main Board	**592**	**856**	**277**	**32**	**33**	**1,790**
6.5.1.1 Main Board	592	856	277	32	33	1,790
Preprocessor	**65**	**262**	**232**	**65**	**0**	**623**
6.5.2.2 Preprocessor	65	262	232	65	0	623
ELMB++MB	**84**	**80**	**90**	**78**	**0**	**332**
6.5.3.3 ELMB++MB	84	80	90	78	0	332
LVPS	**541**	**523**	**124**	**56**	**0**	**1,244**
6.5.2.4 LVPS	397	320	82	0	0	798
6.5.4.4 LVPS Assembly	144	203	42	56	0	446
NSF Grand Total	**1,282**	**1,720**	**723**	**231**	**33**	**3,988**

WBS 6.5 Tile Calorimeter NSF Deliverables Cost AYk$

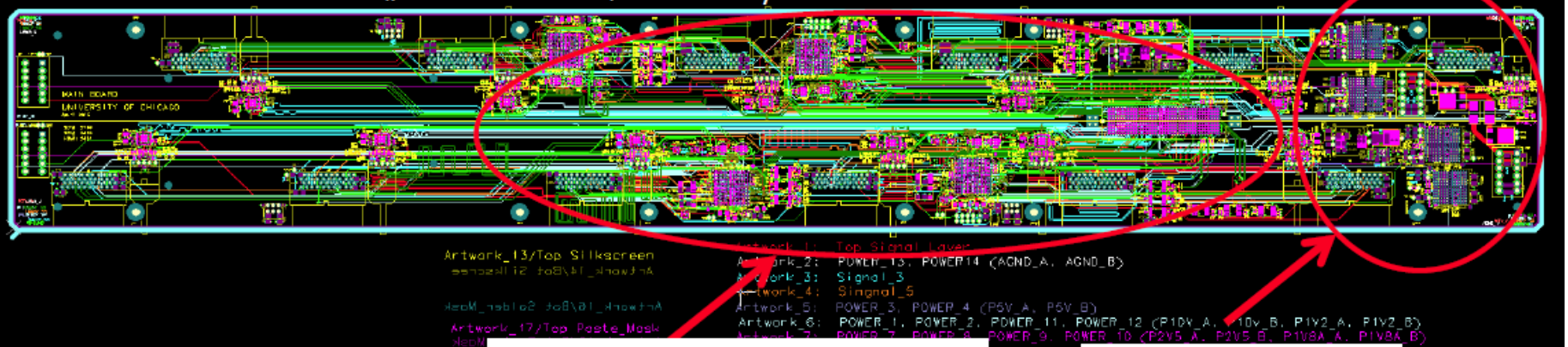


6.5.1.1: Main Board (UC)

- interface between FE amplifier/shaper and fast communications DaughterBoard
- 69 cm length , 16 layer board; 1024 needed
- Supplies LV levels, controls, digitization
- into 3rd prototype version for demonstrator

Complexity and Challenges:

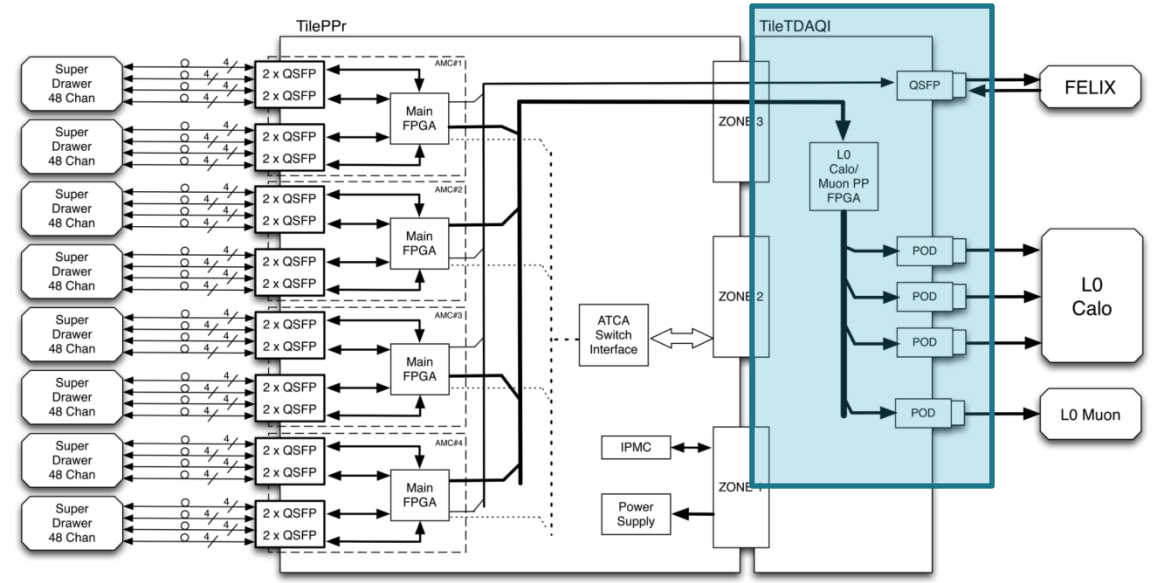
- High speed: (640 Mbps)
- Max. trace length: (20 inches)
- All routes are same direction routes
- Crosstalk consideration: (parallel and tandem)
- Mixed signals (low noise analog and high speed digital)
- Equal timing high speed traces
- Current rate constraints
- Swish-cheesed power planes (via usage limitation)
- Many other constraints



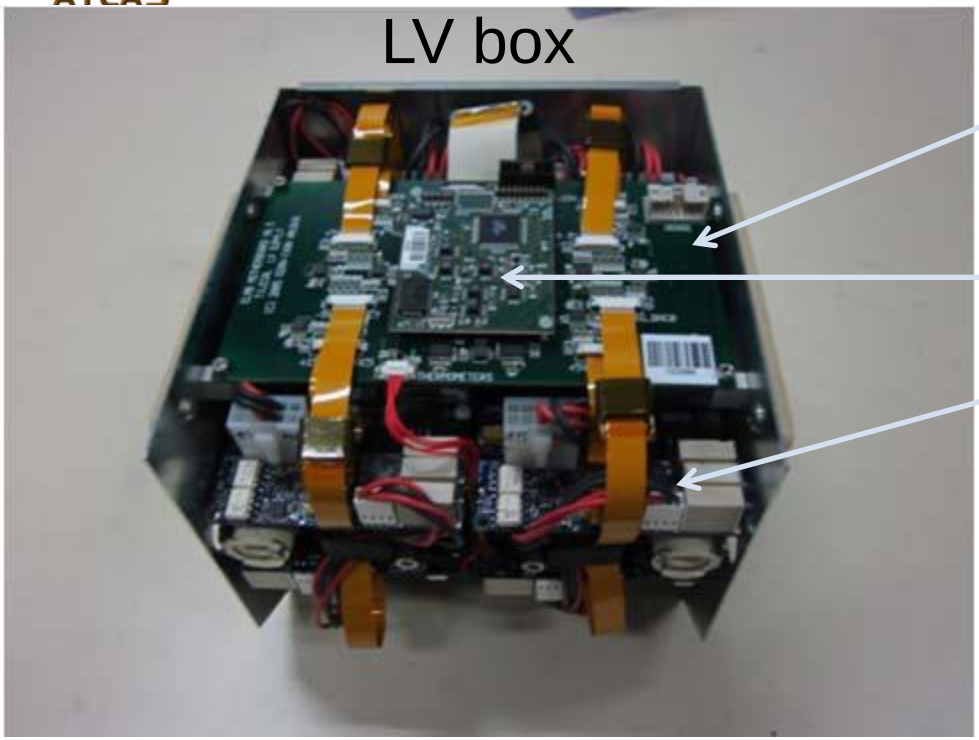
- 6 Signal layers
- 8 Power layers including 3 redundant ground layers (continuous solid plane) for signal integrity and tandem crosstalk reduction

6.5.2.2: Pre-Processor TDAQi (UTA-1)

- PPr + TDAQinterface: receive the ADC raw data, process/calibrate, route data
- TDAQi = smart rear transition module on back-end PreProcessor
  - routes processed cell data to DAQ system
  - send reduced data to trigger processors
- UTA will produce all 32 boards needed
- UTA has long involvement in sROD (PPR) maintenance, debugging
- PPR front-end prototyped for demonstrator; TDAQi designed and costed



6.5.3.3: ELMB++ Motherboard (MSU)



- Motherboard with ELMB handles communication between LVbox and Detector Control System
  - set voltages
  - monitor current, temperature

- MSU proposes to design and make all 256 motherboards needed for LV system
- MSU has had longtime role in Tile control systems
- is starting work with CERN to specify ELMB++ specs

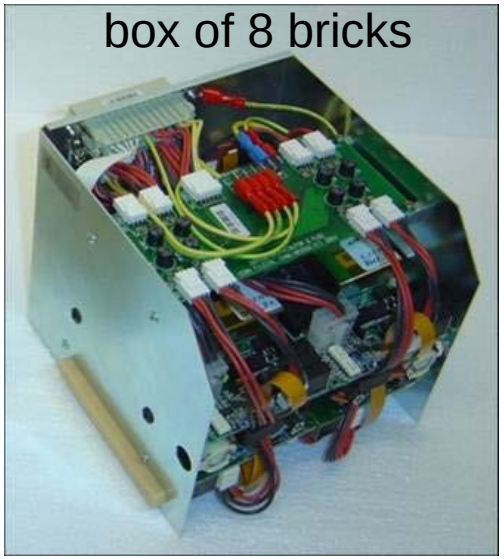
6.5.x.4: LVPS (UTA,NIU)

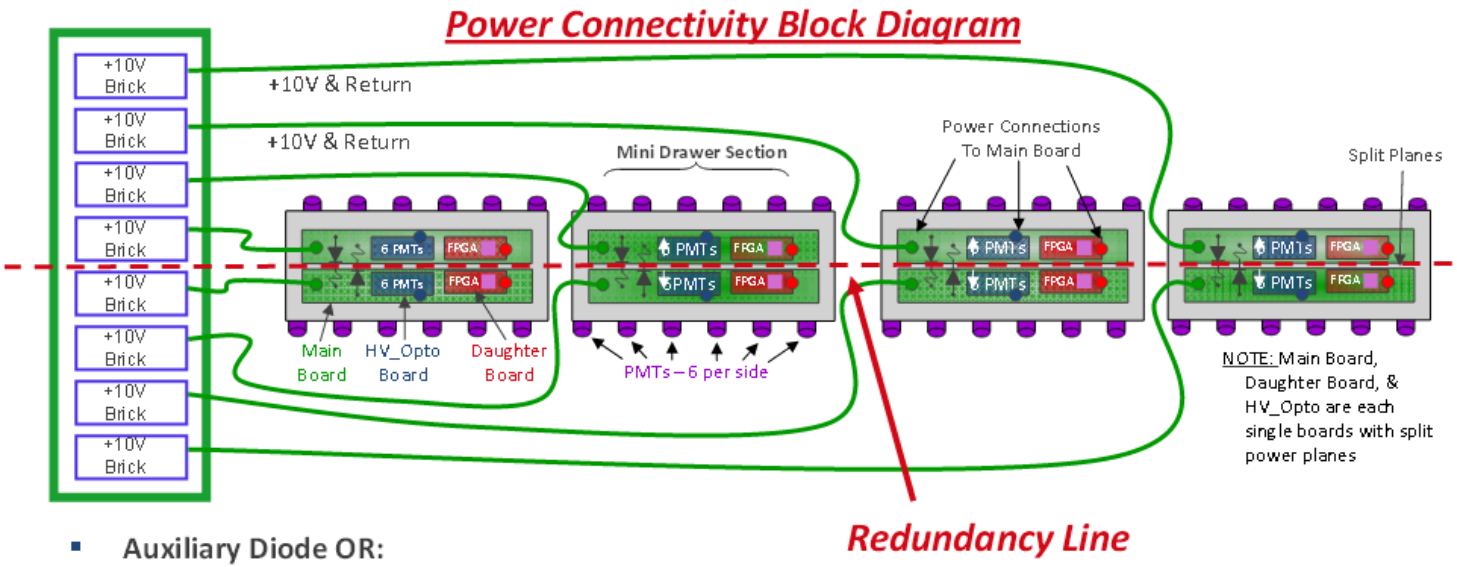
UTA makes 50% of bricks; NIU makes/assembles 50% of boxes

One 10v brick

- Each brick supplies 10v to half of a Main Board
  - feed point of load regulators
- Board fabricated by vendor
- Burned in and tested at UTA
- NIU:
  - makes boxes
  - assembles with bricks
  - attaches ELMB MB
  - tests

box of 8 bricks





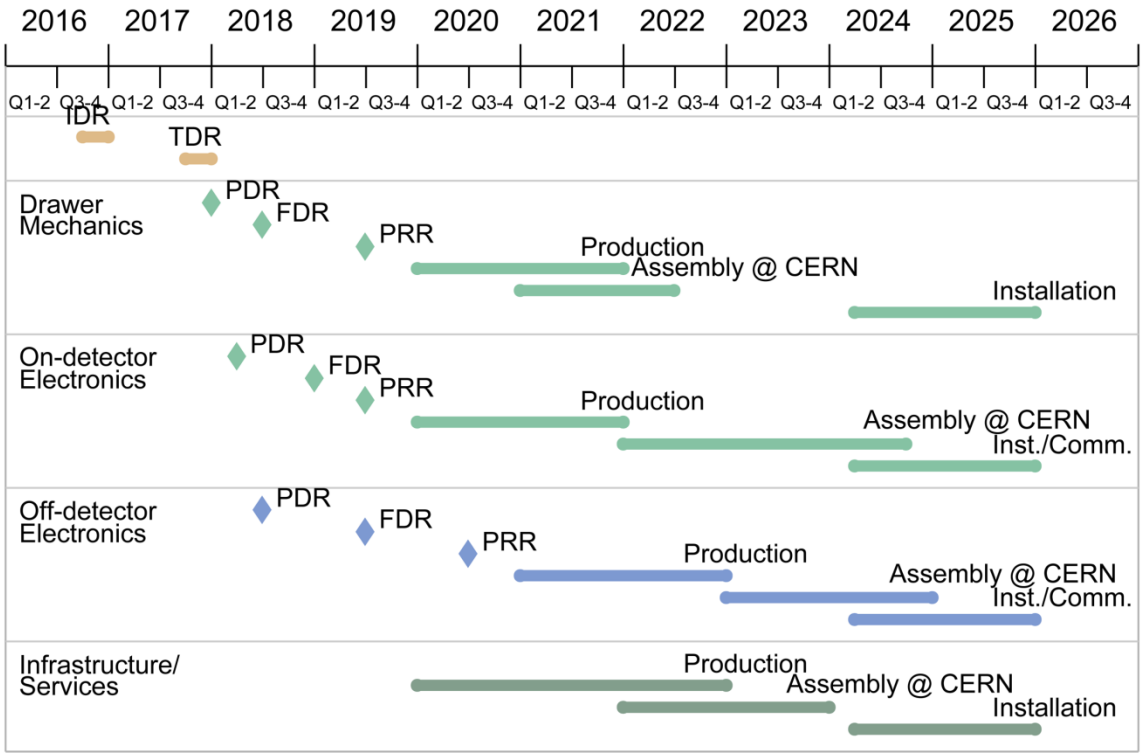
- Auxiliary Diode OR:

Front-end Alternatives:

Pending Downselect

- Chicago's 3in1 FEB and associated Main Board are the **default**
  - Performing well in tests and radiation certification
  - Most complicated MB (has ADCs); total MB cost ≈ total FEB cost
  - Shapes pulse and has dual gain ranges
- Two ASIC alternatives being evaluated
  - QIE (ANL): boxcar integrator, 5 gain ranges
  - FATALIC (LPC Clermont-Ferrand): shaped pulse, 3 gain ranges
  - Downselect: by end of CY 2017
- Whatever alternative is chosen, UChicago and LPC will share:
  - Chicago makes the Main Boards (simpler for the ASIC alternatives)
  - LPC manufactures the front-end cards
    - This makes sense especially if an ASIC is used (single point of contact)

Schedule from Scoping Document



- This was an early exercise
- New “drop dead” dates: 6/30/2024 for all on-barrel electronics
  12/31/2024 for off-detector electronics

6.5 Risk Registry

HL-LHC Upgrade Project Risk Registry for L2 Systems January 4, 2016			Risk Evaluation (L/M/H)							
WBS	**Title**	**Risk Owner**	**Cost**	**Schedule**	**Scope**	**Contingency %**	**Contingency AYk$**	**Average Risk Score**	**Identified Risks (See BoEs)**	
6.5	**Tile Calorimeter**	**Oreglia, Mark**				**35%**	**1,310**	**2.5**		
6.5.1.1	Main Board	Oreglia, Mark	L	L	L	35%	626	2.0	*A higher failure rate necessitating more repair, or increased component costs. *late delivery of parts. *Components no longer radiation qualified	
6.5.2.2	Preprocessor	De, Kaushik	L	L	L	35%	213	2.0	*late delivery of parts. *change in parts costs	
6.5.3.3	ELMB++MB	Huston, J	L	L	L	35%	99	2.0	*late delivery of parts. *The ELMB++ is designed to be standard for all DCS communications	
6.5.x.4	LVPS	Brandt A., Charaborty D.	M	L	L	35%	372	3.0	*Transfer of production (from one institution to another) increases schedule uncertainty. *Labor costs less certain due to lack of experience with this production *Card component no longer rad qualified.	

L3 Total Cost by Institution

6.5 Tile Calorimeter NSF Level 3 Cost (AYk$)						
	FY20	FY21	FY22	FY23	FY24	Grand Total
NSF						
6.5.1 Tile_Chicago	592	856	277	32	33	1,790
6.5.2 Tile_UTA	461	581	313	65	0	1,421
6.5.3 Tile_MSU	84	80	90	78	0	332
6.5.4 Tile_NIU	144	203	42	56	0	446
NSF Total	**1,282**	**1,720**	**723**	**231**	**33**	**3,988**

Effort: FTEs by Task

6.5 Tile Calorimeter NSF Total FTEs by Phase

Deliverable/Item/Phase	FY20	FY21	FY22	FY23	FY24	Grand Total
6.5.1 Tile_Chicago	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
6.5.1.1 Main Board	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
Production Procurement	0.10	0.10	-	-	-	0.20
Production PCB Assembly	0.20	0.20	-	-	-	0.40
Production Burn-in	-	1.80	1.80	-	-	3.60
Production Diagnose & Repair	-	0.20	0.20	-	-	0.40
Ship to CERN	-	0.05	0.10	-	-	0.15
Accceptance Test	-	0.10	0.10	-	-	0.20
Management	-	-	-	0.10	0.10	0.20
6.5.2 Tile_UTA	**2.49**	**3.95**	**2.64**	**0.42**	**-**	**9.50**
6.5.2.2 Preprocessor	**0.26**	**1.44**	**1.36**	**0.42**	**-**	**3.48**
Pre-Prod Parts Procurement/QA	0.04	-	-	-	-	0.04
Pre-Prod PCB Assembly, QA	0.12	-	-	-	-	0.12
Pre-Prod Board Testing	0.10	-	-	-	-	0.10
Parts Procurement/Q&A	-	0.08	0.08	-	-	0.16
PCB Assembly, QA	-	0.08	-	-	-	0.08
Burn-in	-	0.84	0.76	0.16	-	1.76
Repairs	-	0.44	0.52	0.16	-	1.12
Shpping	-	-	-	0.10	-	0.10
6.5.2.4 Low Voltage Power Supply	**2.23**	**2.51**	**1.28**	**-**	**-**	**6.02**
Pre-prod Parts Procurement	0.06	-	-	-	-	0.06
Pre-prod PCB Fab and Assy	0.02	-	-	-	-	0.02
Pre-prod Basic Checkout and Burn-in	0.50	-	-	-	-	0.50
Pre-prod Repairs	0.17	-	-	-	-	0.17
Pre-prod Test Equipment	0.04	-	-	-	-	0.04
Parts Procurement	0.05	0.04	-	-	-	0.09
PCB Fabr & Assy	0.06	0.06	-	-	-	0.13
Basic Checkout & Burn-in	1.21	2.21	1.13	-	-	4.54
Repairs	0.06	0.10	0.10	-	-	0.27
Management	0.04	0.08	0.04	-	-	0.17
Shipping	0.01	0.01	0.01	-	-	0.03
6.5.3 Tile_MSU	**0.45**	**0.37**	**0.47**	**0.35**	**-**	**1.64**
6.5.3.3 ELMB++ Motherboards	**0.45**	**0.37**	**0.47**	**0.35**	**-**	**1.64**
Pre-Prod Burn-in, Test & Repair	0.45	-	-	-	-	0.45
Parts Procurement/Q&A	-	0.06	0.06	-	-	0.11
Burn-in/Test/Repair	-	0.30	0.39	0.32	-	1.01
Shipping	-	0.02	0.02	0.03	-	0.07
6.5.4 Tile_NIU	**0.54**	**0.35**	**0.27**	**0.27**	**-**	**1.42**
6.5.4.4 LVPS Assembly	**0.54**	**0.35**	**0.27**	**0.27**	**-**	**1.42**
Final Design	0.20	-	-	-	-	0.20
Pre-Prod Procurement	0.20	-	-	-	-	0.20
Pre-Prod Assembly	0.05	-	-	-	-	0.05
Pre-Prod Burn-in, Test & Repair	0.05	-	-	-	-	0.05
Pre-Prod Diagnostics & Repair	0.05	-	-	-	-	0.05
Test Equipment	-	0.27	-	-	-	0.27
Production Procurement	-	0.08	-	-	-	0.08
Production Assembly	-	-	0.05	0.02	-	0.07
Production Burn-in/Checkout	-	-	0.14	0.14	-	0.27
Production Diagnose & Repair	-	-	0.09	0.09	-	0.18
Shipping	-	-	-	0.02	-	0.02
NSF Grand Total	**3.78**	**7.12**	**5.59**	**1.14**	**0.10**	**17.72**